# Chapter 6
# IDE BUS INTERFACE AND ATA COMMANDS

This chapter describes the interface between Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives and the IDE bus. The commands that are issued from the host to control the drive are listed, as well as the electrical and mechanical characteristics of the interface.

## 6.1 INTRODUCTION

Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives use the standard IBM PC IDE bus interface, and are compatible with systems that provide an IDE interface connector on the motherboard. It may also be used with a third-party adapter board in systems that do not have a built-in IDE adapter. The adapter board plugs into a standard 16-bit expansion slot in an AT-compatible computer. A cable connects the drive to the adapter board.

## 6.2 SOFTWARE INTERFACE

The Quantum Fireball TM series of drives are controlled by the Basic Input/Output System (BIOS) program residing in an IBM PC AT, or compatible PC. The BIOS communicates directly with the drive's built-in controller. It issues commands to the drive and receives status information from the drive.

## 6.3 MECHANICAL DESCRIPTION

### 6.3.1 Drive Cable and Connector

The hard disk drive connects to the host computer by means of a cable. This cable has a 40-pin connector that plugs into the drive, and a 40-pin connector that plugs into the host computer. At the host end, the cable plugs into either an adapter board residing in a host expansion slot, or an on-board IDE adapter.

If two drives are connected by a cable with two 40-pin drive connectors, the cable-select feature of the Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT drive automatically configures each as either drive 0 or drive 1 depending on the configuration of pin 28 on the connector. See Section 3.3.1, "Cable Select (CS) Jumper," for more information about the cable select jumper.

## 6.4 ELECTRICAL INTERFACE

### 6.4.1 IDE Bus Interface

A 40-pin IDE interface connector on the motherboard or an adapter board provides an interface between the drive and a host that uses an IBM PC AT bus. The IDE interface contains bus drivers and receivers compatible with the standard AT bus. The AT-bus interface signals D8–D15, INTRQ, and IOCS16– require the IDE adapter board to have an extended I/O-bus connector.

The IDE interface buffers data and control signals between the drive and the AT bus of the host system, and decodes addresses on the host address bus. The Command Block Registers on the drive accept commands from the host system BIOS.

Note: Some host systems do not read the Status Register after the drive issues an interrupt. In such cases, the interrupt may not be acknowledged. To overcome this problem, you may have to configure a jumper on the motherboard or adapter board to allow interrupts to be controlled by the drive's interrupt logic. Read your motherboard or adapter board manual carefully to find out how to do this.

#### 6.4.1.1 Electrical Characteristics

All signals are transistor-transistor logic (TTL) compatible—with logic 1 greater than 2.0 volts and less than 5.25 volts; and logic 0 greater than 0.0 volts and less than 0.8 volts. Neither the adapter board, motherboard interface, or drives require terminating resistors.

#### 6.4.1.2 Drive Signals

The drive connector (J1, section C) connects the drive to an adapter board or onboard IDE adapter in the host computer. J1, section C is a 40-pin shrouded connector with two rows of 20 pins on 100-mil centers. J1 has been keyed by removing pin 20. The connecting cable is a 40-conductor flat ribbon cable, with a maximum length of 18 inches.

Table 6-1 describes the signals on the drive connector (J1, section C). The drive does not use all of the signals provided by the IDE bus. Table 6-2 shows the relationship between the drive connector (J1, section C) and the IDE bus.

Note: In Table 6-1, the following conventions apply:

A minus sign follows the name of any signal that is asserted as active low.
Direction (DIR) is in reference to the drive.
IN indicates input to the drive.
OUT indicates output from the drive.
I/O indicates that the signal is bidirectional.

**Table 6-1** *Drive Connector Pin Assignments (J1, Section C)*

| SIGNAL | NAME | DIR | PIN | DESCRIPTION |
|---|---|---|---|---|
| Reset | RESET– | IN | 1 | Drive reset signal from the host system, inverted on the adapter board or motherboard. Asserted for at least 300 ns during start up and deasserted thereafter, unless some event subsequently requires that the drive be reset. |
| Ground | Ground | — | 2 | Ground between the host system and the drive. |
| Data Bus | | I/O | 3–18 | An 8/16-bit, bidirectional data bus between the host and the drive. D0–D7 are used for 8-bit transfers, such as registers and ECC bytes. |
| | DD0 | | 17 | Bit 0 |
| | DD1 | | 15 | Bit 1 |
| | DD2 | | 13 | Bit 2 |
| | DD3 | | 11 | Bit 3 |
| | DD4 | | 9 | Bit 4 |
| | DD5 | | 7 | Bit 5 |
| | DD6 | | 5 | Bit 6 |
| | DD7 | | 3 | Bit 7 |
| | DD8 | | 4 | Bit 8 |
| | DD9 | | 6 | Bit 9 |
| | DD10 | | 8 | Bit 10 |
| | DD11 | | 10 | Bit 11 |
| | DD12 | | 12 | Bit 12 |
| | DD13 | | 14 | Bit 13 |
| | DD14 | | 16 | Bit 14 |
| | DD15 | | 18 | Bit 15 |
| Ground | Ground | — | 19 | Ground between the host system and the drive. |
| Keypin | KEYPIN | — | 20 | Pin removed to key the interface connector. |
| DMA Request | DMARQ | OUT | 21 | Asserted by the drive when it is ready to exchange data with the host. The direction of the data transfer is determined by DIOW– and DIOR–. DMARQ is used in conjunction with DMACK– |
| Ground | Ground | — | 22 | Ground between the host system and the drive. |
| I/O Write | DIOW– | IN | 23 | The rising edge of this write strobe provides a clock for data transfers from the host data bus (DD0–DD7 or DD0–DD15) to a register or to the drive's data port. |
| Ground | Ground | — | 24 | Ground between the host system and the drive. |

**Table 6-1** *Drive Connector Pin Assignments (J1, Section C) (Continued)*

| SIGNAL | NAME | DIR | PIN | DESCRIPTION |
|---|---|---|---|---|
| I/O Read | DIOR– | IN | 25 | The rising edge of this read strobe provides a clock for data transfers from a register or the drive's data port to the host data bus (DD0–DD7 or DD0–DD15). The rising edge of DIOR– latches data at the host. |
| Ground | Ground | — | 26 | Ground between the host system and the drive. |
| I/O Channel Ready | IORDY | OUT | 27 | When the drive is not ready to respond to a data transfer request, the IORDY signal is asserted active low to extend the host transfer cycle of any host register read or write access. When IORDY is deasserted, it is in a high-impedance state and it is the host's responsibility to pull this signal up to a high level (if necessary). |
| Cable Select (Quantum specific) | | — | 28 | This is a Quantum-specific signal from the host that allows the drive to be configured as drive 0 when the signal is 0 (grounded), and as drive 1 when the signal is 1 (high). |
| DMA Acknowledge | DACK1– | IN | 29 | Used by the host to respond to the drive's DMARQ signal. DMARQ signals that there is more data available for the host. |
| Ground | Ground | — | 30 | Ground between the host system and the drive. |
| Interrupt Request | INTRQ | OUT | 31 | An interrupt to the host system. Asserted only when the drive microprocessor has a pending interrupt, the drive is selected, and the host clears nIEN in the Device Control Register. When nIEN is a 1 or the drive is not selected, this output signal is in a high-impedance state, regardless of the presence or absence of a pending interrupt.<br><br>INTRQ is deasserted by an assertion of RESET–, the setting of SRST in the Device Control Register, or when the host writes to the Command Register or reads the Status Register.<br><br>When data is being transferred in programmed I/O (PIO) mode, INTRQ is asserted at the beginning of each data block transfer. Exception: INTRQ is not asserted at the beginning of the first data block transfer that occurs when any of the following commands executes: FORMAT TRACK, Write Sector, WRITE BUFFER, or WRITE LONG. |
| 16-Bit I/O | IOCS16– | OUT | 32 | An open-collector output signal. Indicates to the host system that the 16-bit data port has been addressed and that the drive is ready to send or receive a 16-bit word. When transferring data in PIO mode, if IOCS16– is not asserted, D0–D7 are used for 8-bit transfers; if IOCS16– is asserted, D0–D15 are used for 16-bit data transfers. |

**Table 6-1** *Drive Connector Pin Assignments (J1, Section C) (Continued)*

| SIGNAL | NAME | DIR | PIN | DESCRIPTION |
|---|---|---|---|---|
| Drive Address Bus | | | | A 3-bit, binary-coded address supplied by the host when accessing a register or the drive's data port. |
| Bit 1 | DA1 | IN | 33 | |
| Bit 0 | DA0 | IN | 35 | |
| Bit 2 | DA2 | IN | 36 | |
| | | | | |
| Passed Diagnostics | PDIAG– | I/O | 34 | Drive 0 (Master) monitors this Drive 1 (Slave) open-collector output signal, which indicates the result of a diagnostics command or reset. Each drive has a 10K pull-up resistor on this signal.<br><br>Following the receipt of a power-on reset, software reset, or RESET– drive 1 negates PDIAG– within 1 ms. PDIAG– indicates to drive 0 that drive 1 is busy (BSY=1). Then, drive 1 asserts PDIAG– within 30 seconds, indicating that drive 1 is no longer busy (BSY=0) and can provide status information. Following the assertion of PDIAG–, drive 1 is unable to accept commands until drive 1 is ready (DRDY=1)—that is, until the reset procedure for drive 1 is complete.<br><br>Following the receipt of a valid EXECUTE DRIVE DIAGNOSTIC command, drive 1 negates PDIAG– within 1 ms, indicating to drive 0 that it is busy and has not yet passed its internal diagnostics. If drive 1 is present, drive 0 waits for drive 1 to assert PDIAG– for up to 5 seconds after the receipt of a valid EXECUTE DRIVE DIAGNOSTIC command. Since PDIAG– indicates that drive 1 has passed its internal diagnostics and is ready to provide status, drive 1 clears BSY prior to asserting PDIAG–.<br><br>If drive 1 fails to respond during reset initialization, drive 0 reports its own status after completing its internal diagnostics. Drive 0 is unable to accept commands until drive 0 is ready (DRDY=1)—that is, until the reset procedure for drive 0 is complete. |
| Chip Select 0 | CS1FX– | IN | 37 | Chip-select signal decoded from the host address bus. Used to select the host-accessible Command Block Registers. |
| Chip Select 1 | CS3FX– | IN | 38 | Chip select signal decoded from the host address bus. Used to select the host-accessible Control Block Registers. |

**Table 6-1** *Drive Connector Pin Assignments (J1, Section C) (Continued)*

| SIGNAL | NAME | DIR | PIN | DESCRIPTION |
|---|---|---|---|---|
| Drive Active/Slave Present | DASP– | I/O | 39 | A time-multiplexed signal that indicates either drive activity or that drive 1 is present. During power-on initialization, DASP– is asserted by drive 1 within 400 ms to indicate that drive 1 is present. If drive 1 is not present, drive 0 asserts DASP– after 450 ms to light the drive-activity LED.<br><br>An open-collector output signal, DASP– is deasserted following the receipt of a valid command by drive 1 or after the drive is ready, whichever occurs first. Once DASP– is deasserted, either hard drive can assert DASP– to light the drive-activity LED. Each drive has a 10K pull-up resistor on this signal.<br><br>If an external drive-activity LED is used to monitor this signal, an external resistor must be connected in series between the signal and a +5 volt supply in order to limit the current to 24 mA maximum. |
| Ground | Ground | — | 40 | Ground between the host system and the drive. |

#### 6.4.1.3 IDE Bus Signals

See Table 6-2 for the relationship between the drive signals and the IDE bus.

**Table 6-2** *Relationship of Drive Signals to the IDE Bus*

| DRIVE CONNECTOR (J1) | | DIRECTION | IDE BUS | |
|---|---|---|---|---|
| 1 | RESET– | <—(INV) | B2 | RESET DRV |
| 2 | GROUND | — | — | GROUND |
| 3 | DD7 | <—> | A2 | SD7 |
| 4 | DD8 | <—> | C11 | SD8 |
| 5 | DD6 | <—> | A3 | SD6 |
| 6 | DD9 | <—> | C12 | D9 |
| 7 | DD5 | <—> | A4 | SD5 |
| 8 | DD10 | <—> | C13 | SD10 |
| 9 | DD4 | <—> | A5 | SD4 |
| 10 | DD11 | <—> | C14 | SD11 |
| 11 | DD3 | <—> | A6 | SD3 |
| 12 | DD12 | <—> | C15 | SD12 |
| 13 | DD2 | <—> | A7 | SD2 |
| 14 | DD13 | <—> | C16 | SD13 |
| 15 | DD1 | <—> | A8 | SD1 |
| 16 | DD14 | <—> | C17 | SD14 |
| 17 | DD0 | <—> | A9 | SD0 |
| 18 | DD15 | <—> | C18 | SD15 |
| 19 | GROUND | — | — | GROUND |
| 20 | KEYPIN | — | — | NO CONNECTION |
| 21 | DMARQ | —> | —[1] | DRQ |
| 22 | GROUND | — | — | GROUND |
| 23 | DIOW– | <— | B13 | DIOW– |
| 24 | GROUND | — | — | GROUND |
| 25 | DIOR– | <— | B14 | IOR– |
| 26 | GROUND | — | — | GROUND |
| 27 | IORDY | —> | A10 | I/O CH RDY |
| 28 | CABLE SELECT | <— | —[2] | NO CONNECTION |
| 29 | DMACK– | <— | —[3] | DACK– |
| 30 | GROUND | — | — | GROUND |
| 31 | INTRQ | —> | D7 | INTRQ |
| 32 | IOCS16– | —> | D2 | I/O CS16– |
| 33 | ADDR1 | <— | A30 | SA1 |
| 34 | PDIAG– | — | — | NO CONNECTION |
| 35 | DA0 | <— | A31 | SA0 |
| 36 | ADDR2 | <— | A29 | SA2 |
| 37 | CS1FX– | <— | —[4] | CS0– |
| 38 | CS3FX– | <— | —[4] | CS1– |
| 39 | DASP– | — | —[4] | NO CONNECTION |
| 40 | GROUND | — | — | GROUND |

1. DMARQ from the drive must be jumpered to one of the DRQ lines on the motherboard or host adapter (normally connected to DRQ6).
2. Pin 28 is a vendor-specific pin that Quantum is using for a specific purpose. See Chapter 3 for details.
3. DACK– from the drive must be jumpered to one of the DACK– lines on the motherboard or host adapter (normally connected to DACK6–).
4. CS1FX–, CS3FX–, and DASP– originate on the adapter board.

## 6.4.2 Host Interface Timing

### 6.4.2.1 Programmed I/O (PIO) Transfer Mode

The PIO host interface timing shown in Table 6-3 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-1 provides a timing diagram.

**Table 6-3** *PIO Host Interface Timing*

| SYMBOL | DESCRIPTION | MIN/MAX | MODE 4[1] (local bus) | QUANTUM FIREBALL TM AT |
|---|---|---|---|---|
| t0 | Cycle Time | min | 120 | 120 |
| t1 | Address Valid to DIOW–/DIOR–Setup | min | 25 | 25 |
| t2 | DIOW–/DIOR– Pulsewidth (8- or 16-bit) | min | 70 | 70 |
| t2i | DIOW–/DIOR– Negated Pulsewidth | min | 25 | 25 |
| t3 | DIOW–Data Setup | min | 20 | 20 |
| t4 | DIOW– Data Hold | min | 10 | 10 |
| t5 | DIOR– Data Setup | min | 20 | 20 |
| t5a | DIOR– to Data Valid | max | — | — |
| t6 | DIOR– Data Hold | min | 5 | 5 |
| t6z | DIOR– Data Tristate | max | 30 | 30 |
| t7 | Address Valid to IOCS16– Assertion | max | N/A | N/A |
| t8 | Address Valid to IOSC16– Deassertion | max | N/A | N/A |
| t9 | DIOW–/DIOR– to Address Valid Hold | min | 10 | 10 |
| tA | IORDY[2] Setup Time | min | 35 | 35 |
| tB | IORDY Pulse Width | max | 1250 | 1250 |
| tR | Read Data Valid to IORDY active (if IORDY is initially low after tA) | min | 0 | 0 |

1. ATA Mode 4 timing is listed for reference only.
2. Transfer rates above 6 MB/s require the use of IORDY.

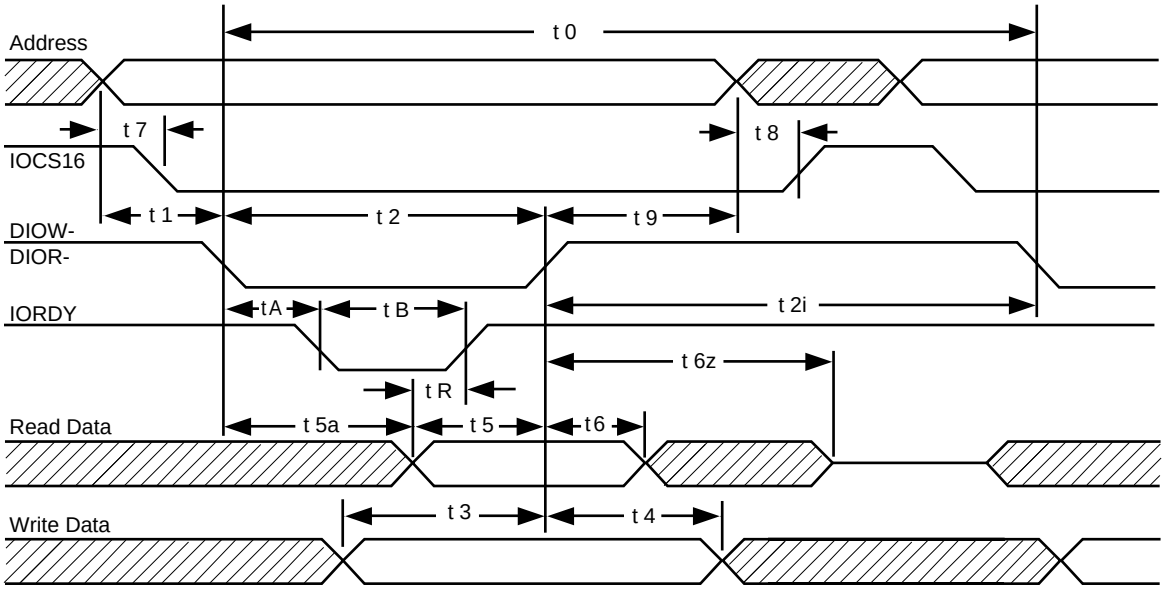


**Figure 6-1** *PIO Interface Timing*

#### 6.4.2.2 Multiword DMA Transfer Mode

The multiword DMA host interface timing shown in Table 6-4 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-2 provides a timing diagram.

**Table 6-4** *Multiword DMA Host Interface Timing*

| SYMBOL | DESCRIPTION | MIN/MAX | MODE 2[1] (local bus) | QUANTUM FIREBALL TM AT |
|---|---|---|---|---|
| t0 | Cycle Time | min | 120 | 120 |
| tD | DIOR–/DIOW– Pulsewidth | min | 70 | 70 |
| tE | DIOR– to Data Valid | max | – | – |
| tF | DIOR– Data Hold | min | 5 | 5 |
| tFz | DIOR– Data Tristate[2] | max | 20 | 20 |
| tG | DIOW– Data Setup | min | 20 | 20 |
| tH | DIOW– Data Hold | min | 10 | 10 |
| tI | DMACK to DIOR–/DIOW– Setup | min | 0 | 0 |
| tJ | DIOR–/DIOW– to DMACK– Hold | min | 5 | 5 |
| tK | DIOR–/DIOW– Negated Pulsewidth | min | 25 | 25 |
| tL | DIOR–/DIOW– to DMARQ Delay | max | 35 | 35 |
| tz | DMACK– Data Tristate[3] | max | 25 | 25 |

1. ATA Mode 2 timing is listed for reference only.
2. The Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT drive tristates after each word transferred.
3. Symbol tz only applies on the last tristate at the end of a multiword DMA transfer cycle.

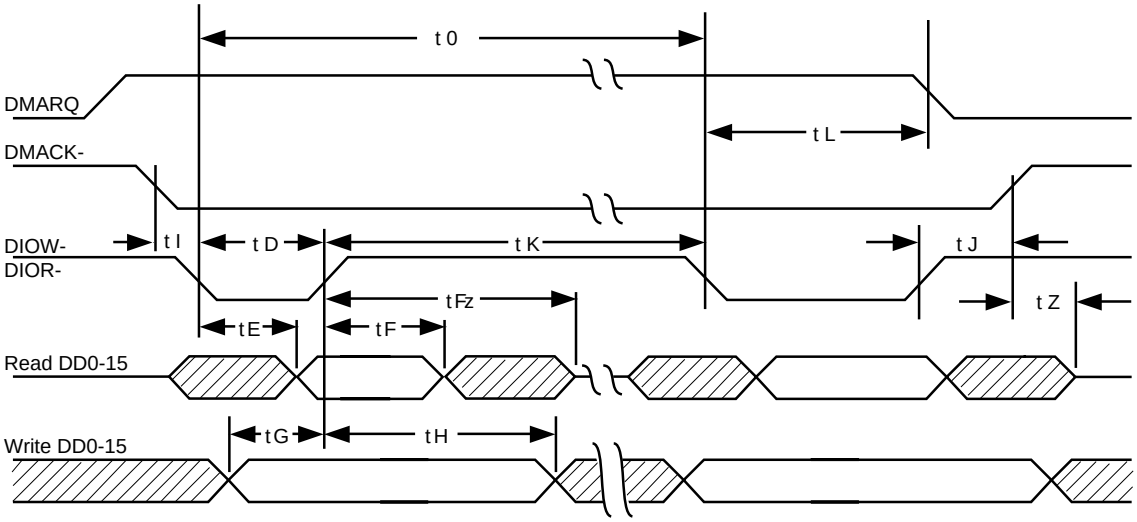


**Figure 6-2** *Multiword DMA Bus Interface Timing*

### 6.4.2.3 Host Interface RESET Timing

The host interface RESET timing shown in Table 6-5 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-3 provides a timing diagram.

**Table 6-5** *Host Interface RESET Timing*

| SYMBOL | DESCRIPTION | MINIMUM | MAXIMUM |
|---|---|---|---|
| tM | RESET– Pulse width | 300 | — |

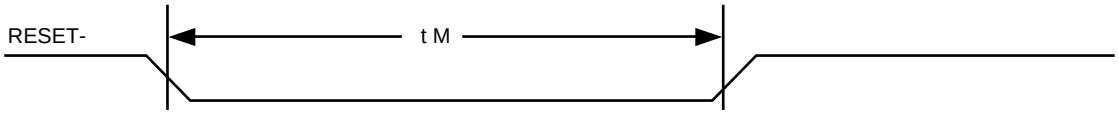


**Figure 6-3** *Host Interface RESET Timing*

## 6.5 REGISTER ADDRESS DECODING

The host addresses the drive by using programmed I/O. Host address lines A0–A2, chip-select CS1FX– and CS3FX–, and IOR– and IOW– address the disk registers. Host address lines A3–A9 generate the two chip-select signals, CS1FX– and CS3FX–.

- Chip Select CS1FX– accesses the eight Command Block Registers.
- Chip Select CS3FX– is valid during 8-bit transfers to or from the Alternate Status Register.

The drive selects the primary or secondary command block addresses by setting Address bit A7.

Data bus lines 8–15 are valid only when IOCS16– is active and the drive is transferring data. The drive transfers ECC information only on data bus lines 0–7. Data bus lines 8–15 are invalid during transfers of ECC information.

I/O to or from the drive occurs over an I/O port that routes input or output data to or from selected registers, by using the following encoded signals from the host: CS1FX–, CS3FX–, DA2, DA1, DA0, DIOR–, and DIOW–. The host writes to the Command Block Registers when transmitting commands to the drive, and to the Control Block Registers when transmitting control, like a software reset. Table 6-6 lists the selection addresses for these registers.

**Table 6-6** *I/O Port Functions and Selection Addresses*

| FUNCTION | | HOST SIGNALS | | | | |
|---|---|---|---|---|---|---|
| **CONTROL BLOCK REGISTERS** | | **CS1FX–** | **CS3FX–** | **DA2** | **DA1** | **DA0** |
| **READ (DIOR–)** | **WRITE (DIOW–)** | | | | | |
| Data Bus High Impedance | Not Used | N[1] | N | X[2] | X | X |
| Data Bus High Impedance | Not Used | N | A[3] | 0 | X | X |
| Data Bus High Impedance | Not Used | N | A | 1 | 0 | X |
| Alternate Status | Device Control | N | A | 1 | 1 | 0 |
| Drive Address | Not Used | N | A | 1 | 1 | 1 |
| **COMMAND BLOCK REGISTERS** | | | | | | |
| **READ (DIOR–)** | **WRITE (DIOW–)** | | | | | |
| Data Port | Data Port | A | N | 0 | 0 | 0 |
| Error Register | Features | A | N | 0 | 0 | 1 |
| Sector Count | Sector Count | A | N | 0 | 1 | 0 |
| Sector Number[4] | Sector Number | A | N | 0 | 1 | 1 |
| LBA Bits 0–7[5] | LBA Bits 0–7 | A | N | 0 | 1 | 1 |
| Cylinder Low[4] | Cylinder Low | A | N | 1 | 0 | 0 |
| LBA Bits 8–15[5] | LBA Bits 8–15 | A | N | 1 | 0 | 0 |
| Cylinder High[4] | Cylinder High | A | N | 1 | 0 | 1 |
| LBA Bits 16–23[5] | LBA Bits 16–23 | A | N | 1 | 0 | 1 |
| Drive/Head[4] | Drive/Head | A | N | 1 | 1 | 0 |
| LBA Bits 24–27[5] | LBA Bits 24–27 | A | N | 1 | 1 | 0 |
| Status | Command | A | N | 1 | 1 | 1 |
| Invalid Address | Invalid Address | A | A | X | X | X |

1. N = signal deasserted
2. X = signal either asserted or deasserted
3. A = signal asserted
4. Mapping of registers in CHS mode
5. Mapping of registers in LBA mode

After power on or following a reset, the drive initializes the Command Block Registers to the values shown in Table 6-7.

**Table 6-7** *Command Block Register Initial Values*

| REGISTER | VALUE |
|---|---|
| Error Register | 01 |
| Sector Count Register | 01 |
| Sector Number Register | 01 |
| Cylinder Low Register | 00 |
| Cylinder High Register | 00 |
| Drive/Head Register | 00 |

## 6.6 REGISTER DESCRIPTIONS

The Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives emulate the ATA Command and Control Block Registers. Functional descriptions of these registers are given in the next two sections.

### 6.6.1 Control Block Registers

#### 6.6.1.1 Alternate Status Register

The Alternate Status Register contains the same information as the Status Register in the command block. Reading the Alternate Status Register does not imply the acknowledgment of an interrupt by the host or clear a pending interrupt. See the description of the Status Register in section 6.6.2.8 for definitions of bits in this register.

#### 6.6.1.2 Device Control Register

This write-only register contains two control bits, as shown in Table 6-8.

**Table 6-8** *Device Control Register Bits*

| BIT | MNEMONIC | DESCRIPTION |
|---|---|---|
| 7 | Reserved | – |
| 6 | Reserved | – |
| 5 | Reserved | – |
| 4 | Reserved | – |
| 3 | 1 | Always 1 |
| 2 | SRST[1] | Host software reset bit |
| 1 | nIEN[2] | Drive interrupt enable bit |
| 0 | 0 | Always 0 |

1. SRST = Host Software Reset bit. When the host sets this bit, the drive is reset. When two drives are daisy-chained on the interface, this bit resets both drives simultaneously.
2. nIEN = Drive Interrupt Enable bit. When nIEN equals 0 or the host has selected the drive, the drive enables the host interrupt signal INTRQ through a tristate buffer to the host. When nIEN equals 1 or the drive is not selected, the host interrupt signal INTRQ is in a high-impedance state, regardless of the presence or absence of a pending interrupt.

#### 6.6.1.3 Drive Address Register

The Drive Address Register returns the head-select addresses for the drive currently selected. Table 6-9 shows the Drive Address bits.

**Table 6-9** *Drive Address Register Bits*

| BIT | MNEMONIC | DESCRIPTION |
|---|---|---|
| 7 | HiZ[1] | High Impedance bit |
| 6 | nWTG[2] | Write Gate bit |
| 5 | nHS3[3] | Head Address msb |
| 4 | nHS2 | – |
| 3 | nHS1 | – |
| 2 | nHS0 | Head Address lsb |
| 1 | nDS1[4] | Drive 1 Select bit |
| 0 | nDS0 | Drive 0 Select bit |

1. HiZ = High Impedance bit. When the host reads the register, this bit will be in a high impedance state.
2. nWTG = Write Gate bit. When a write operation to the drive is in progress, nWTG equals 0.
3. nHS0–nHS3 = Head Address bits. These bits are equivalent to the one's complement of the binary-coded address of the head currently selected.
4. nDS0–nDS1 = Drive Select bits. When drive 1 is selected, nDS1 equals 0. When drive 0 is selected, nDS0 equals 0.

### 6.6.2 Command Block Registers

#### 6.6.2.1 Data Port Register

All data transferred between the device data buffer and the host passes through the Data Port Register. The host transfers the sector table to this register during execution of the FORMAT TRACK command. Transfers of ECC bytes during the execution of READ LONG or WRITE LONG commands are 8-bit transfers.

#### 6.6.2.2 Error Register

The Error Register contains status information about the last command executed by the drive. The contents of this register are valid only when the Error bit (ERR) in the Status Register is set to 1. The contents of the Error Register are also valid at power on, and at the completion of the drive's internal diagnostics, when the register contains a status code. When the error bit in the Status Register is set to 1, the host interprets the Error Register bits as shown in Table 6-10.

**Table 6-10** *Error Register Bits*

| MNEMONIC | BIT | DESCRIPTION |
|---|---|---|
| BBK | 7 | Bad block detected in the required sector's ID field. |
| UNC | 6 | Uncorrectable data error encountered. |
| – | 5 | Not used. |
| IDNF | 4 | Requested sector's ID field not found. |
| – | 3 | Not used. |
| ABRT | 2 | Requested command aborted due to a drive status error, such as Not Ready or Write Fault, or because the command code is invalid. |
| TK0NF | 1 | Track 0 not found during execution of RECALIBRATE command. |
| AMNF | 0 | Data Address Mark not found after correct ID field format. |

#### 6.6.2.3 Sector Count Register

The Sector Count Register defines the number of sectors of data to be transferred across the host bus for a subsequent command. If the value in this register is 0, the sector count is 256 sectors. If the Sector Count Register command executes successfully, the value in this register at command completion is 0. As the drive transfers each sector, it decrements the Sector Count Register to reflect the number of sectors remaining to be transferred. If the command's execution is unsuccessful, this register contains the number of sectors that must be transferred to complete the original request.

When the drive executes an INITIALIZE DRIVE PARAMETERS or Format Track command, the value in this register defines the number of sectors per track.

#### 6.6.2.4 Sector Number Register

The Sector Number Register contains the ID number of the first sector to be accessed by a subsequent command. The sector number is a value between one and the maximum number of sectors per track. As the drive transfers each sector, it increments the Sector Number Register. See the command descriptions in section 6.7 for information about the contents of the Sector Number Register after successful or unsuccessful command completion.

In LBA mode, this register contains bits 0 to 7. At command completion, the host updates this register to reflect the current LBA bits 0 to 7.

#### 6.6.2.5 Cylinder Low Register

The Cylinder Low Register contains the eight low-order bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register when command execution is complete, to reflect the current cylinder number. The host loads the least significant bits of the cylinder address into the Cylinder Low Register.

In LBA mode, this register contains bits 8 to 15. At command completion, the host updates this register to reflect the current LBA bits 8 to 15.

#### 6.6.2.6 Cylinder High Register

The Cylinder High Register contains the eight high-order bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register at the completion of command execution, to reflect the current cylinder number. The host loads the most significant bits of the cylinder address into the Cylinder High Register.

In LBA mode, this register contains bits 16 to 23. At command completion, the host updates this register to reflect the current LBA bits 16 to 23.

#### 6.6.2.7 Drive/Head Register

The Drive/Head Register contains the drive ID number and its head numbers. By executing the INITIALIZE DRIVE PARAMETERS command, the host defines the contents of the Drive/Head Register.

In LBA mode, this register contains bits 24 to 27. At command completion, the host updates this register to reflect the current LBA bits 24 to 27.

Table 6-11 shows the Drive/Head Register bits.

**Table 6-11** *Drive Head Register Bits*

| MNEMONIC | BIT | DESCRIPTION |
|---|---|---|
| Reserved | 7[1] | Always *1* |
| L | 6[2] | *0* for CHS mode<br>*1* for LBA mode |
| Reserved | 5 | Always *1* |
| DRV | 4[3] | *0* indicates the Master drive is selected<br>*1* indicates the Slave drive is selected |
| HS3 | 3[4] | Most significant Head Address bit in CHS mode<br>Bit 24 of the LBA Address in LBA mode |
| HS2 | 2 | Head Address bit for CHS mode<br>Bit 25 of the LBA Address in LBA mode |
| HS1 | 1 | Head Address bit for CHS mode<br>Bit 26 of the LBA Address in LBA mode |
| HS0 | 0 | Least significant Head Address bit in CHS mode<br>Bit 27 of the LBA Address in LBA mode |

1. Bits 5–7 define the sector size set in hardware (512 bytes).
2. Bit 6 is the binary encoded Address Mode Select. When bit 6 is set to 0, addressing is by CHS mode. When bit 6 is set to 1, addressing is by LBA mode.
3. Bit 4 (DRV) contains the binary encoded drive select number. The Master is the primary drive; the Slave is the secondary drive
4. In CHS mode, bits 3–0 (HS0–HS3) contain the binary encoded address of the selected head. At command completion, the host updates these bits to reflect the address of the head currently selected. In LBA mode, bits 3–0 (HS0–HS3) contain bits 24–27 of the LBA Address. At command completion, the host updates this register to reflect the current LBA bits 24 to 27.

#### 6.6.2.8 Status Register

The Status Register contains information about the status of the drive and the controller. The drive updates the contents of this register at the completion of each command. When the Busy bit is set (BSY=1), no other bits in the Command Block Registers are valid. When the Busy bit is not set (BSY=0), the information in the Status Register and Command Block Registers is valid.

When an interrupt is pending, the drive considers that the host has acknowledged the

interrupt when it reads the Status Register. Therefore, whenever the host reads this register, the drive clears any pending interrupt. Table 6-12 defines the Status Register bits.

#### 6.6.2.9 Command Register

The host sends a command to the drive by means of an 8-bit code written to the Command Register. As soon as the drive receives the command in its Command Register, it begins execution of the command. Table 6-13 lists the hexadecimal command codes and parameters for each executable command. The code F0h is common to all of the extended commands. Each of these commands is distinguished by a unique subcode. For a detailed description of each command, see Section 6.7, "COMMAND DESCRIPTIONS," found later in this chapter.

**Table 6-12** *Status Register Bits*

| MNEMONIC | BIT | DESCRIPTION |
|---|---|---|
| BSY | 7 | **Busy bit**. Set by the controller logic of the drive whenever the drive has access to, and the host is locked out of the Command Block Registers.<br>BSY is set under the following conditions:<br>• Within 400 ns after the deassertion of RESET- or after SRST is set in the Device Control Register. Following a reset, BSY will be set for no longer than 30 seconds.<br>• Within 400 ns of a host write to the Command Block Registers with a Read, READ LONG, READ BUFFER, SEEK, RECALIBRATE, INITIALIZE DRIVE PARAMETERS, Read Verify, Identify Drive, or EXECUTE DRIVE DIAGNOSTIC command.<br>• Within 5 μsec after the transfer of 512 bytes of data during the execution of a Write, Format Track, or WRITE BUFFER command, or 512 bytes of data and the appropriate number of ECC bytes during the execution of a WRITE LONG command.<br>When BSY=1, the host cannot write to a Command Block Register and reading any Command Block Register returns the contents of the Status Register. |
| DRDY | 6 | **Drive Ready bit**. Indicates that the drive is ready to accept a command. When an error occurs, this bit remains unchanged until the host reads the Status Register, then again indicates that the drive is ready. At power on, this bit should be cleared, and should remain cleared until the drive is up to speed and ready to accept a command. |
| DWF | 5 | **Drive Write Fault bit.** When an error occurs, this bit remains unchanged until the host reads the Status Register, then again indicates the current write fault status. |
| DSC | 4 | **Drive Seek Complete bit.** This bit is set when a seek operation is complete and the heads have settled over a track. When an error occurs, this bit remains unchanged until the host reads the Status Register, when it indicates the current seek-complete status. |
| DRQ | 3 | **Data Request bit.** When set, this bit indicates that the drive is ready to transfer a word or byte of data from the host to the data port. |
| CORR | 2 | **Corrected Data bit.** The drive sets this bit when it encounters and corrects a correctable data error. This condition does not terminate a multisector read operation. |
| IDX | 1 | **Index bit.** This bit is set when the drive detects the index mark, once per disk revolution. |
| ERR | 0 | **Error bit.** When set, this bit indicates that the previous command resulted in an error. The other bits in the Status Register and the bits in the Error Register contain additional information about the cause of the error. |

**Table 6-13** *Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT drive Command Codes and Parameters*

| COMMAND | | PARAMETER | | | | |
|---|---|---|---|---|---|---|
| NAME | CODE | SC | SN | CY | DS | HD |
| RECALIBRATE | 1Xh | | | | V | |
| READ SECTORS, with retry | 20h | V | V | V | V | V |
| READ SECTORS, no retry | 21h | V | V | V | V | V |
| READ LONG, with retry | 22h | V | V | V | V | V |
| READ LONG, no retry | 23h | V | V | V | V | V |
| WRITE SECTORS, with retry | 30h | V | V | V | V | V |
| WRITE SECTORS, no retry | 31h | V | V | V | V | V |
| WRITE LONG, with retry | 32h | V | V | V | V | V |
| WRITE LONG, no retry | 33h | V | V | V | V | V |
| READ VERIFY SECTORS, with retry | 40h | V | V | V | V | V |
| READ VERIFY SECTORS, no retry | 41h | V | V | V | V | V |
| FORMAT TRACK | 50h | V | | V | V | V |
| SEEK | 7Xh | | V | V | V | V |
| EXECUTE DRIVE DIAGNOSTIC | 90h | | | | | |
| INITIALIZE DRIVE PARAMETERS | 91h | V | | | V | V |
| READ MULTIPLE | C4h | V | V | V | V | V |
| WRITE MULTIPLE | C5h | V | V | V | V | V |
| SET MULTIPLE MODE | C6h | V | | | V | |
| READ DMA, with retry | C8h | V | V | V | V | V |
| READ DMA, no retry | C9h | V | V | V | V | V |
| WRITE DMA, with retry | CAh | V | V | V | V | V |
| WRITE DMA, no retry | CBh | V | V | V | V | V |
| STANDBY IMMEDIATE | E0h | | | | | V |
| IDLE IMMEDIATE | E1h | | | | | V |
| STANDBY MODE (AUTO POWER-DOWN) | E2h | V | | | | V |
| IDLE MODE (AUTO POWER-DOWN) | E3h | V | | | | V |
| READ BUFFER | E4h | | | | V | |
| CHECK POWER MODE | E5h | V | | | | V |
| SLEEP MODE | E6h | | | | | V |
| WRITE BUFFER | E8h | | | | V | |
| IDENTIFY DRIVE | ECh | | | | V | |
| READ DEFECT LIST—extended cmnd. | F0h | V | V | V | V | V |
| READ CONFIGURATION—extended cmnd. | F0h | V | V | V | V | V |
| SET CONFIGURATION—extended cmnd. | F0h | V | V | V | V | V |

Note: The following information applies to Table 6-13:
SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Low and High Registers
DS = Drive Select bit (Bit 4 of Drive/Head Register)
HD = 3 Head Select Bits (Bits 0–3 of Drive Head Register)
V = Must contain valid information for this command

## 6.7 COMMAND DESCRIPTIONS

The Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives support all standard ATA drive commands. The drive decodes, then executes, commands loaded into the Command Block Register. In applications involving two hard drives, both drives receive all commands. However, only the selected drive executes commands—with the exception of the EXECUTE DRIVE DIAGNOSTIC command, as explained below. The procedure for executing a command on the selected drive is as follows:

1. Wait for the drive to indicate that it is no longer busy (BSY=0).
2. Load the required parameters into the Command Block Register.
3. Activate the Interrupt Enable (–IEN) bit.
4. Wait for the drive to set RDY (RDY=1).
5. Write the command code to the Command Register.

Execution of the command begins as soon as the drive loads the Command Block Register. The remainder of this section describes the function of each command. The commands are listed in the same order they appear in Table 6-13.

### 6.7.1 Recalibrate 1xh

The RECALIBRATE command moves the read/write heads from any location on the disk to cylinder 0. On receiving this command, the drive sets the BSY bit and issues a seek command to cylinder 0. The drive then waits for the seek operation to complete, updates status, negates BSY, and generates an interrupt. If the drive cannot seek to cylinder 0, it posts the message TRACK 0 NOT FOUND.

### 6.7.2 Read Sectors 20h (with retry), 21h (without retry)

The Read Sectors command reads from 1 to 256 sectors, beginning at the specified sector. As specified in the Command Block Register, a sector count equal to 0 requests 256 sectors. When the drive accepts this command, it sets BSY and begins execution of the command.

#### 6.7.2.1 Read Long 22h (with retry), 23h (without retry)

When the Long bit is set in the command code, a READ LONG command executes, returning the data and the ECC bytes contained in the data field of the requested sector. During a READ LONG operation, the drive does not check the ECC bytes to determine if a data error of any kind has occurred.

#### 6.7.2.2 Multiple Sector Reads

Multiple sector reads set DRQ. After reading each sector, the drive generates an interrupt when the sector buffer is full, and the drive is ready for the host to read the data. Once the host empties the sector buffer, the drive immediately clears DRQ and sets BSY.

If an error occurs during a multiple sector read, the read terminates at the sector in which the error occurred. The Command Block Register contains the cylinder, head, and sector numbers of the sector in which the error occurred. The host can then read the Command Block Register to determine what kind of error has occurred, and in which sector. Whether the data error is correctable or uncorrectable, the drive loads the data into the sector buffer.

### 6.7.3 Write Sector 30h (with retry), 31h (without retry)

The WRITE SECTOR command writes from 1 to 256 sectors, beginning at the specified sector. As specified in the Command Block Register, a sector count equal to 0 requests 256 sectors. When the drive accepts this command, it sets DRQ and waits for the host to fill the sector buffer with the data to be written to the drive. The drive does not generate an interrupt to start the first buffer-fill operation. Once the buffer is full, the drive clears DRQ, sets BSY, and begins execution of the command.

#### 6.7.3.1 Write Long 32h (with retry), 33h (without retry)

When the Long bit is set in the command code, a WRITE LONG command writes the data and the ECC bytes directly from the sector buffer. The drive does not generate the ECC bytes itself.

#### 6.7.3.2 Multiple Sector Writes

The MULTIPLE SECTOR WRITES command sets DRQ. The drive generates an interrupt whenever the sector buffer is ready to be filled. When the host fills the sector buffer, the drive immediately clears DRQ and sets BSY.

If an error occurs during a multiple sector write operation, the write operation terminates at the sector in which the error occurred. The Command Block Register contains the cylinder, head, and sector numbers of the sector in which the error occurred. The host can then read the Command Block Register to determine what kind of error has occurred, and in which sector.

### 6.7.4 Read Verify Sectors 40h (with retry), 41h (without retry)

The execution of the READ VERIFY SECTORS command is identical to that of the READ SECTORS command. However, the Read Verify command does not cause the drive to set DRQ, the drive transfers no data to the host, and the Long bit is invalid. On receiving the READ VERIFY command, the drive sets BSY. When the drive has verified the requested sectors, it clears BSY and generates an interrupt. On command completion, the Command Block Registers contain the cylinder, head, and sector numbers of the last sector verified.

If an error occurs during a multiple sector verify operation, the read operation terminates at the sector in which the error occurred. The Command Block Registers contain the cylinder, head, and sector numbers in which the error occurred.

### 6.7.5 Format Track 50h

The host specifies the track addresses by writing to the Cylinder and Head Registers. When the drive accepts a FORMAT TRACK command, it sets the DRQ bit, then waits for the host to fill the sector buffer. When the buffer is full, the drive clears DRQ, sets BSY, and begins command execution. The contents of the sector buffer are not written to the disk, and may be ignored or interpreted as shown in Table 6-14.

**Table 6-14** *Sector Buffer Contents*

| DD15 --- DD0 | | DD15 --- DD0 | |
|---|---|---|---|
| First Sector Descriptor | :: :::::::::::: | Last Sector Descriptor | Remainder of buffer filled with zeros |

On the Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drive, the FORMAT TRACK command writes zeros to the data fields in the sectors on the specified logical track. The drive writes no headers at these locations. The Sector Count register contains the number of sectors per track.

One 16-bit word represents each sector (the words are contiguous from the start of the sector).

Note: Any words remaining in the buffer after the representation of the last sector must be filled with zeros.

DD15–8 contain the sector number. DD7–0 contain a descriptor value that is defined below. The words must appear in sequential order starting at sector one and ending on the last sector number of the track.

- 00h Format sector as good
- 20h Unassign the alternate location for this sector
- 40h Assign this sector to an alternate location
- 80h Format sector as bad

### 6.7.6 Seek 7xh

The SEEK command causes the actuator to seek the track to which the Cylinder and Drive/Head registers point. When the drive receives this command in its Command Block Registers, it performs the following functions:

1. Sets BSY
2. Initiates the seek operation
3. Resets BSY
4. Sets the Drive Seek Complete (DSC) bit in the Status Register

The drive does not wait for the seek to complete before it sends an interrupt. If the BSY bit is *not* set in the Status Register, the drive can accept and queue subsequent commands while performing the seek. If the Cylinder registers contain an illegal cylinder, the drive sets the ERR bit in the Status Register and the IDNF bit in the Error Register.

### 6.7.7 Execute Drive Diagnostic 90h

The EXECUTE DRIVE DIAGNOSTIC command performs the internal diagnostic tests implemented on the drive. Drive 0 sets BSY within 400 ns of receiving of the command.

If Drive 1 is present:

- Both drives execute diagnostics.
- Drive 0 waits up to six seconds for drive 1 to assert PDIAG–.
- If drive 1 does not assert PDIAG– to indicate a failure, drive 0 appends 80h with its own diagnostic status.
- If the host detects a drive 1 diagnostic failure when reading drive 0 status, it sets the DRV bit, then reads the drive 1 status.

If Drive 1 is not present:

- Drive 0 reports only its own diagnostic results.
- Drive 0 clears BSY and generates an interrupt.

If drive 1 fails diagnostics, drive 0 appends 80h with its own diagnostic status and loads that code into the Error Register. If drive 1 passes its diagnostics or no drive 1 is present, drive 0 appends 00h with its own diagnostic status and loads that code into the Error Register.

The diagnostic code written to the Error Register is a unique 8-bit code. Table 6-15 lists the diagnostic codes.

**Table 6-15** *Diagnostic Codes*

| DIAGNOSTIC CODE | DESCRIPTION |
|---|---|
| 01h | No Error Detected |
| 02h | Formatter Device Error |
| 03h | Sector Buffer Error |
| 04h | ECC Circuitry Error |
| 05h | Controlling Microprocessor Error |
| 8Xh | Drive 1 Failed |

### 6.7.8 Initialize Drive Parameters 91h

The INITIALIZE DRIVE PARAMETERS command enables the host to set the logical number of heads and the logical number of sectors per track. On receiving the command, the drive sets the BSY bit, saves the parameters, clears BSY, and generates an interrupt.

The only two register values used by this command are the Sector Count Register, which specifies the number of sectors; and the Drive/Head Register, which specifies the number of heads, minus 1. The DRV bit assigns these values to drive 0 or drive 1, as appropriate.

This command does not check the sector count and head values for validity. If these values are invalid, the drive will not report an error until another command causes an illegal access.

### 6.7.9 Read Multiple C4h

The execution of the READ MULTIPLE command is identical to that of the Read Sectors command. However, the READ MULTIPLE command:

- Transfers blocks of data to the host without intervening interrupts
- Requires DRQ qualification of the transfer only at the start of the block—*not* at each sector
- Invalidates the Long bit

The SET MULTIPLE MODE command specifies the block count, or the number of sectors to be transferred as a block. This command executes prior to the READ MULTIPLE command. When the host issues a READ MULTIPLE command, the Sector Count Register contains the number of sectors requested—not the number of blocks or the block count.

If this sector count is not evenly divisible by the block count, the drive transfers as many full blocks as possible to the host, followed by a final partial-block transfer. The partial-block transfer is for *n* sectors, where:

n = (sector count) module (block count)

If the drive attempts execution of a READ MULTIPLE command before executing the SET MULTIPLE MODE command, or if READ MULTIPLE commands are disabled, an abort command error occurs.

The drive reports disk errors encountered during READ MULTIPLE commands at the beginning of a block or partial-block transfer. However, the drive still sets DRQ and transfers the data—including any corrupted data.

### 6.7.10 Write Multiple C5h

The execution of the WRITE MULTIPLE command is identical to that of the Write Sectors command. However, the WRITE MULTIPLE command:

- Causes the controller to set BSY within 400 ns of accepting the command
- Causes the drive to transfer multiple-sector blocks of data to the drive without intervening interrupts
- Requires DRQ qualification of the transfer only at the start of the block, not at each sector
- Invalidates the Long bit

The SET MULTIPLE MODE command specifies the block count, or the number of sectors to be transferred as a block. This command executes prior to the WRITE MULTIPLE command. When the host issues a WRITE MULTIPLE command, the Sector Count Register contains the number of sectors requested—not the number of blocks or the block count.

If this sector count is not evenly divisible by the block count, the drive transfers as many full blocks as possible, followed by a final partial-block transfer. The partial-block transfer is for *n* sectors, where:

*n* = (sector count) module (block count)

If the drive attempts to execute a WRITE MULTIPLE command before executing the SET MULTIPLE MODE command, or while WRITE MULTIPLE commands are disabled, an Abort Command error occurs.

During the execution of a WRITE MULTIPLE command, the drive reports all disk errors encountered, following an attempted disk write of the block or partial block. When an error occurs, the WRITE MULTIPLE command ends at the sector that contains the error—even if it is in the middle of a block—and does not transfer subsequent blocks. The drive generates interrupts by setting DRQ at the beginning of each block or partial block.

### 6.7.11 Set Multiple Mode C6h

The SET MULTIPLE MODE command enables the controller to perform READ MULTIPLE and WRITE MULTIPLE operations, and establishes the block count for these commands.

Prior to issuing a command, the host should load the Sector Count Register with the number of sectors per block. On receiving this command, the drive sets BSY and checks the contents of the Sector Count Register.

If the Sector Count Register contains a valid value, and the controller supports block count, the controller loads the values for all subsequent READ MULTIPLE and WRITE MULTIPLE commands, and enables execution of these commands. Any unsupported block count in the register causes an Aborted Command error, and disables execution of READ MULTIPLE and WRITE MULTIPLE commands.

If the Sector Count Register contains a zero value when the host issues the command, READ MULTIPLE and WRITE MULTIPLE commands are disabled. Any unsupported block count in the register causes an aborted command error, and disables READ MULTIPLE and WRITE MULTIPLE commands. After the command is executed, the controller clears BSY. At power on, or after a software or hardware reset, the default mode for the READ MULTIPLE and WRITE MULTIPLE commands is disabled.

### 6.7.12 Read Buffer E4h

The READ BUFFER command enables the host to read the current contents of the drive's sector buffer. When the host issues this command, the drive sets BSY, sets up the sector buffer for a read operation, sets DRQ, class BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the buffer.

The drive can synchronize READ BUFFER and WRITE BUFFER commands from the host; that is, sequential READ BUFFER and WRITE BUFFER commands can access the same 512 bytes within the buffer.

### 6.7.13 Write Buffer E8h

The WRITE BUFFER command allows the host to write the first 512 bytes of the drive's buffer. On receiving this command in its Command Block Register, the drive sets BSY and prepares for a write operation. When ready, the drive sets DRQ, resets BSY, and generates INTRQ, allowing the host to the buffer.

### 6.7.14 Power Management Commands

The Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives provide numerous management options. Two important options center around a count down counter known as the automatic power down counter or APD. This counter can trigger one of two power saving events depending on which of the two commands was most recently issued.

- Standby: Once a standby command is issued, the drive enters the standby mode. Further, each time the APD counter reaches zero in the future, the drive enters the standby mode, the spindle and actuator motors are off and the heads are parked in the landing zone. Receipt of any command that requires media access causes the drive to exit the standby command and service the host request. Each time the drive executes the standby command, the drive will reenter the standby mode when the APD counter reaches zero.
- Idle: Once an idle command is issued, each time the APD counter reaches zero, the drive enters the standby mode. In the standby mode, the actuator and spindle motors are off with the heads locked in the landing area. This is the default setting.
- Automatic Power Down (APD) Mode: When in APD mode, the drive transitions to standby mode when the APD time elapses. Receipt of any command that requires media access causes the drive to exit standby mode. Upon receiving a command, the drive resets the APD counter to zero and starts it again (with the exception of the Check Power Mode Command, which does not reset the APD counter).

Three commands are available which are not dependent upon the APD counter reaching zero:

- Sleep: When a sleep command is received, the drive enters the sleep mode. In the sleep mode, the spindle and actuator motors are off and the heads are latched in the landing zone. Receipt of a reset causes the drive to transition from the sleep to the standby mode.
- Standby Immediate: When a standby immediate command is received, the drive immediately enters the standby mode.
- Idle Immediate: When an idle immediate command is received, after the first decrement of the APD counter, the drive enters the idle mode.

The sleep, standby immediate, and idle immediate commands differ in a significant way from the standby and idle commands. Specifically, sleep, standby immediate, and idle immediate have a one-time effect and must be reissued each time their effect is desired. In contrast, standby and idle operate in conjunction with the APD counter and stay in effect continually, becoming non-effectual only upon issuance of the other of these two commands. Thus, for example, once the standby command is issued just one time, each time the APD counter reaches zero the drive will enter the standby mode.

Note: The user has the ability to determine the value to which the APD counter is set upon completion of any command. This value is set by writing to the Sector Count Register a number between 12 and 255 just prior to issuance of a standby or idle command. Each increment represents a five-second time interval.

#### 6.7.14.1 Standby Immediate Mode – E0h

The Standby Immediate Mode power command immediately puts the drive in the Standby Mode. Power is removed from the spindle motor (the drive's PCB power remains) and the heads are parked.

#### 6.7.14.2 Idle Immediate Mode – E1h

The Idle Immediate Mode power command immediately puts the drive in the Idle Mode.

#### 6.7.14.3 Standby Mode, Automatic Power-Down – E2h

The Standby Mode, Automatic Power-Down (APD) command immediately puts the drive in the Standby Mode. The Sector Count Register is then examined. If the value in this register is not zero, the Auto Power-Down feature is enabled and will take effect once the countdown timer reaches zero. The valid count range is Table 6-16. Each time the drive is accessed, the countdown timer is reset to the value originally set in the Sector Count Register at the time the Standby Mode-Auto Power Down command was issued.

Note: If the value in the Sector Count Register is zero, the Auto Power-Down feature is disabled.

**Table 6-16** *Valid Count Range*

| SECTOR COUNT | TIME |
|---|---|
| 1 to 12 | 1 minute |
| 13 to 240 | (Value * 5) seconds |
| 241 to 251 | (Value – 240) * 30 seconds |
| 252 to 255 | (Value * 5) seconds |

#### 6.7.14.4 Idle Mode, Automatic Power-Down – E3h

The Idle Mode, Automatic Power-Down command immediately puts the drive into the Idle Mode. The Sector Count Register is then examined. If the value in this register is not zero, the Auto Power-Down feature is enabled and takes effect once the countdown timer reaches zero. The valid count range is listed in Table 6-16. Each time the drive is accessed, the countdown timer is reset to the value originally set in the Sector Count Register at the time the Idle Mode-Auto Power Down command was issued.

Note: If the value in the Sector Count Register is zero, the Auto Power-Down feature is disabled.

#### 6.7.14.5 Check Power Mode – E5h

The CHECK POWER MODE command writes FFh into the Sector Count Register provided that the drive is in the Idle Mode, even if it is in Automatic Power-Down mode. However, if it is in Standby mode, the drive returns a value of 00h in the Sector Count Register.

#### 6.7.14.6 Sleep Mode – E6h

The Quantum Fireball TM drive considers the Sleep Mode to be the equivalent of the Standby Mode, except that a reset is required before issuing a command requiring media access.

### 6.7.15 Identify Drive

The IDENTIFY DRIVE command enables the host to receive parameter information from the drive. When the host issues this command, the drive sets BSY, stores the required parameter information in the sector buffer, sets DRQ, and generates an interrupt. The host then reads the information from the sector buffer. The Identify Drive Parameters Table, shown in Table 6-17, defines the parameter words stored in the buffer. All reserved bits should be zeros. A full explanation of the parameter words is listed below:

**Default Logical Cylinders:** The number of translated cylinders in the default translation mode.

**Number of Logical Heads:** The number of translated heads in the default translation mode.

**Number of Unformatted Bytes Per Track**: The number of unformatted bytes per translated track in the default translation mode.

**Number of Unformatted Bytes Per Sector:** The number of unformatted bytes per sector in the default translation mode.

**Number of Logical Sectors Per Track:** The number of sectors per track in the default translation mode.

**Serial Number:** The contents of this field are left aligned and padded with spaces (20h).

**Buffer Type:** The contents of this field are as follows:

- 0000h = Not specified
- 0001h = A single-ported, single-sector buffer capable of data transfers either to or from the host or to or from the disk
- 0002h = A dual-ported, multiple-sector buffer capable of simultaneous data transfers either to and from the host, or from the host and the disk
- 0003h = A dual-ported, multiple-sector buffer capable of simultaneous data transfers with read caching
- 0004 – FFFFh = Reserved

**Firmware Revision:** The contents of this field are left-aligned and padded with spaces (20h).

**Model Number:** The contents of this field are left-aligned and padded with spaces (20h). The low-order byte appears first in a word.

**Table 6-17** *Identify Drive Parameters*

| WORDS[1] | | | PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1) |
|---|---|---|---|
| WORD | BIT | BIT VALUE | |
| 0 | 15 | 0 | Reserved for nonmagnetic drives |
| | 14 | 0 | Format speed tolerance gap required |
| | 13 | 0 | Track offset option available |
| | 12 | 0 | Data strobe offset option available |
| | 11 | 0 | Rotational speed tolerance is > 0.5% |
| | 10 | 1 | Disk transfer rate > 10 Mbit/s |
| | 9 | 0 | Disk transfer rate > 5 Mbit/s, but < 10 Mbit/s |
| | 8 | 0 | Disk transfer rate <= 5 Mbit/s |
| | 7 | 0 | Reserved for removable-cartridge drive |
| | 6 | 1 | Hard disk drive |
| | 5 | 0 | Spindle motor control option implemented |
| | 4 | 1 | Head-switch time > 15 µs |
| | 3 | 1 | Not MFM-encoded |
| | 2 | 0 | Soft-sectored |
| | 1 | 1 | Hard-sectored |
| | 0 | 0 | Reserved |
| 1 | | 1080AT = 2,112<br>1280AT = 2,484<br>1700AT = 3,309<br>2110AT = 4,092<br>2550AT = 4,969<br>3200AT = 6,232<br>3840AT = 7,480 | Default logical cylinders |
| 2 | | 0 | Reserved |
| 3 | | 1080AT = 16<br>1280AT = 16<br>1700AT = 16<br>2110AT = 16<br>2550AT = 16<br>3200AT = 16<br>3840AT = 16 | Default number of logical heads |
| 4 | | Zone dependent | Number of unformatted bytes per track |
| 5 | | 512 | Number of unformatted bytes per sector |

| WORDS[1] | | | PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1) |
|---|---|---|---|
| **WORD** | **BIT** | **BIT VALUE** | |
| 6 | | 1080AT = 63<br>1280AT = 63<br>1700AT = 63<br>2110AT = 63<br>2550AT = 63<br>3200AT = 63<br>3840AT = 63 | Default number of logical sectors per track |
| 7–9 | | 5154h | Vendor-unique |
| 10–19 | | | Serial number (20 ASCII characters)[2] |
| 20 | | 3 | Buffer type |
| 21 | | 99h | Buffer size in 512-byte increments |
| 22 | | 4 | Number of ECC bytes passed on READ/WRITE LONG commands |
| 23–26 | | | Firmware revision (8 ASCII characters) |
| 27–46 | | | Model number (40 ASCII characters) |
| 47 | 15–8<br>7–0 | 80h<br>10h | Vendor Unique<br>Maximum number of sectors that can be transferred per interrupt is set to 8 for READ MULTIPLE and WRITE MULTIPLE commands. |
| 48 | | 0 | Cannot perform double word I/O |
| 49 | 15–12<br>11<br>10<br>9<br>8<br>7–0 | 0<br>1<br>1<br>1<br>1<br>0 | Reserved<br>1 = I/O Ready is supported<br>1 = I/O Ready can be disabled<br>1 = LBA supported<br>1 = DMA supported<br>Vendor Unique |
| 50 | | 0 | Reserved |
| 51 | 15–8<br>7–0 | 4<br>0 | PIO data-transfer cycle timing mode<br>Vendor Unique |
| 52 | 15–8<br>7–0 | 2<br>0 | DMA data-transfer cycle timing mode<br>Vendor Unique |
| 53 | 15–2<br>1<br>0 | 0<br>1<br>1 | Reserved<br>1 = The fields in words 64–70 are valid<br>1 = The fields in words 54–58 are valid |
| 54 | | | Number of current cylinders |
| 55 | | | Number of current heads |
| 56 | | X | Number of current sectors per track |
| 57–58 | | X | Current capacity in sectors (CHS mode only) |

| WORDS[1] | | | PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1) |
|---|---|---|---|
| **WORD** | **BIT** | **BIT VALUE** | |
| 59 | 15–9<br>8<br>7–0 | 0<br>1<br>n[3] | Reserved<br>Multiple sector setting is valid<br>Current setting for number of sectors that can be transferred per interrupt on R/W Multiple commands |
| 60–61 | | 1080AT = 2,128,896<br>1280AT = 2,503,872<br>1700AT = 3,335,472<br>2110AT = 4,124,736<br>2550AT = 5,008,752<br>3200AT = 6,281,856<br>3840AT = 7,539,840 | Total number of User Addressable Sectors (LBA Mode only) |
| 62 | 15–8<br>7–0 | 4<br>7 | Single-word DMA transfer mode active (Mode 2)<br>Single-word DMA transfer modes supported (Mode 2) |
| 63 | 15–8<br>7–0 | 4<br>7 | Multiword DMA transfer mode active (Mode 2)<br>Multiword DMA transfer modes supported (Mode 2) |
| 64 | | 3 | Advanced PIO Mode is supported |
| 65 | | 120 | Minimum multiword DMA transfer cycle time (ns) per word |
| 66 | | 120 | Manufacturer's recommended multiword DMA cycle time (ns) |
| 67 | | 300 | Manufacturer's PIO cycle time (ns) without flow control |
| 68 | | 120 | Manufacturer's PIO cycle time (ns) with flow control |

1. The format of an ASCII field specifies that, within a word boundary, the low-order byte appears first.
2. The serial number has the following format: 00QTMTCYJJJLSSSSBBB
   where: 00 = Placeholders
   QT = Quantum
   M = Place of manufacture
   TC = Drive type family, and capacity (98 = 1080MB, 97 = 1280MB, 93 = 1700MB, 99 = 2110MB, 94 = 2550MB, 95 = 3200MB, 96 = 3840)
   Y = Last digit of year drive built
   JJJ = Julian date
   L = Manufacturing production line
   SSSS = Sequence of manufacture
   BBB = Blanks (placeholders)
3. n is a variable from zero to 8.

### 6.7.16 Set Features EFh

The SET FEATURES command is used by the host to establish certain parameters which control execution of the following drive features:

- 02h – Enable write cache feature
- 03h – Set transfer mode based on value in Sector Count Register
- 55h – Disable read look-ahead feature
- 82h – Disable write cache feature
- AAh – Enable read look-ahead feature

At power-on, or after a reset accomplished by either the hardware or software, the default mode is 4 bytes of ECC, read look-ahead, and write cache enabled.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode, Disable IORDY00000 001
Single Word DMA Mode x00010 nnn
Multiword DMA Mode x00100 nnn

Where “nnn” is a valid mode number for the associated transfer type.

### 6.7.17 Read Defect List

The READ DEFECT LIST command enables the host to retrieve the drive’s defect list. Prior to issuing the Read Defect List command the host should issue the Read Defect List Length command. This command will not transfer any data. It instead stores the length in sectors of the defect list in the Sector Count register (1F2), and the Sector Number register (1F3), with the Sector Count register containing the LSB of the 2-byte value (see Table 6-18). The defect list length is a fixed value for each Quantum product and can be calculated as follows:

length in sectors = (((maximum number of defects) * 8 + 4) + 511)/512

At the completion of the command, the task file registers 1F2 – 1F6 will contain bytes necessary to execute the Read Defect List command, and the host will only need to write the extended command code (F0h) to the Command register (1F7) to proceed with the Read Defect List command execution.

**Table 6-18** *READ DEFECT LIST LENGTH Command Bytes*

| ADDRESS | VALUE (Before) | DEFINITION | VALUE (After) |
|---|---|---|---|
| 1F2 | 0 | Defect List Subcode | Length in Sectors (LSB) |
| 1F3 | FFh | Password | Length in Sectors (MSB) |
| 1F4 | FFh | Password | FFh |
| 1F5 | 3Fh | Password | 3Fh |
| 1F6 | AXh (Drive 0) | Drive Select | AXh = Drive 0 |
| | BXh (Drive 1) | — | BXh = Drive 1 |
| 1F7 | F0h | Extended Command Code | Status Register |

Note: Registers 1F2h through 1F5h must contain the exact values shown. These values function as a key. The drive issues the message ILLEGAL COMMAND if the bytes are not entered correctly.

The AT Read Defect List command is an extended AT command that enables the host to retrieve the drive's defect list. The host begins by writing to address 1F6h to select the drive. Then the host writes to addresses 1F2h – 1F5h using values indicated in Table 6-19. When the host subsequently writes the extended command code F0h to address 1F7h, the drive sets BSY, retrieves the defect list, sets DRQ, and resets BSY. The host can now read the requested number of sectors (512 bytes) of data. An INTRQ precedes each sector. Bytes 1F2h and 1F3h contain the 2-byte number of sectors that the host expects o read, with address 1F2h containing the LSB (see Table 6-19). The sector count (1F2h – 1F3h) may vary from product to product and if the wrong value is supplied for a specific product, the drive will issue the ILLEGAL COMMAND message. If the host does not know the appropriate sector count for a specific product, it can issue the Read Defect List Length command, described in the previous section to set up the task file for the Read Defect List command.

**Table 6-19** *AT READ DEFECT LIST Command Bytes*

| ADDRESS | VALUE | DEFINITION |
|---|---|---|
| 1F2 | Length in Sectors (LSB) | Defect List Subcode |
| 1F3 | Length in Sectors (MSB) | Defect List Subcode |
| 1F4 | FFh | Password |
| 1F5 | 3Fh | Password |
| 1F6 | AXh = Drive 0 | Drive Select |
| | BXh = Drive 1 | — |
| 1F7 | F0h | Extended Command Code |

Note: Registers 1F2h and 1F3h must contain the transfer length that is appropriate for the specific product, and 1F4h and 1F5h must contain the exact values shown. These values function as a key. The drive issues the message ILLEGAL COMMAND if the bytes are not entered correctly.

Pending defects will be excluded from the list, since no alternate sector is being used as their replacement, and since they may be removed from the drive's internal pending list at a later time. Table 6-20 shows the overall format of the defect list, and Table 6-21 shows the format of the individual defect entries.

**Table 6-20** *DEFECT LIST DATA FORMAT*

| BYTE | DESCRIPTION |
|---|---|
| 0 | 0 |
| 1 | 1Dh |
| 2 | 8* (Number of Defects) (MSB) |
| 3 | 8* (Number of Defects) (LSB) |
| 4–11 | Defect Entry #1 |
| 12–19 | Defect Entry #2 |
| | • |
| | • |

**Table 6-21** *DEFECT ENTRY DATA FORMAT*

| BYTE | DESCRIPTION |
|---|---|
| 0 | Defect cylinder (MSB) |
| 1 | Defect cylinder |
| 2 | Defect cylinder (LSB) |
| 3 | Defect head |
| 4 | Defect sector (MSB) |
| 5 | Defect sector |
| 6 | Defect sector |
| 7 | Defect sector (LSB) |

Note: Bytes 4 – 7 will be set to FFh for bad track entries.

## 6.7.18 Configuration

In addition to the SET FEATURES command, the Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives provide two configuration commands:

- The SET CONFIGURATION command, which enables the host to change DisCache and Error Recovery parameters
- The READ CONFIGURATION command, which enables the host to read the current configuration status of the drive

See Chapter 5 for more details about DisCache and setting cache parameters. See Chapter 5 also for more information about error detection and defect management.

### 6.7.18.1 Read Configuration

The READ CONFIGURATION command displays the configuration of the drive. Like the SET CONFIGURATION command, this command is secured to prevent accidentally accessing it. To access the READ CONFIGURATION command, you must write the pattern shown inTable 6-22 to the Command Block Registers. The first byte, 01h, is a subcode to the extended command code, F0h.

**Table 6-22** *Accessing the READ CONFIGURATION Command*

| ADDRESS | VALUE | DEFINITION |
|---|---|---|
| 1F2h | 01h | Read Configuration Subcode |
| 1F3h | FFh | Password |
| 1F4h | FFh | Password |
| 1F5h | 3Fh | Password |
| 1F6h | AXh (Drive 0) | Drive Select |
| | BXh (Drive 1) | Drive Select |
| 1F7h | F0h | Extended Command Code |

Note: In Table 6-22:

Only the value in address 1F2h of the Command Block Registers is different from the SET CONFIGURATION command.

Registers 1F2h through 1F5h must contain the exact values shown in Table 6-22. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.

To select the drive for which the configuration is to be read, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

A 512-byte data field is associated with the READ CONFIGURATION command. A 512-byte read sequence sends this data from the drive to the host. The information in this data field represents the current settings of the configuration parameters. The format of the READ CONFIGURATION command data field is similar to that for the data field of the SET CONFIGURATION command, shown in Table 6-23. However, in the READ CONFIGURATION command, bytes 0 through 31 of the data field are *not* KEY information, as they are in the SET CONFIGURATION command. The drive reads these bytes as *QUANTUM CONFIGURATION*, followed by eleven spaces. Users can read the configuration into a buffer, then alter the configuration parameter settings.

### 6.7.18.2 Set Configuration – FEh

The SET CONFIGURATION command is secured to prevent accessing it accidentally. To access the SET CONFIGURATION command, you must write the pattern shown in Table 6-23 to the Command Block Registers. The first byte, FFh, is a subcode to the extended command code F0h.

**Table 6-23** *Accessing the SET CONFIGURATION Command*

| ADDRESS | VALUE | DEFINITION |
|---|---|---|
| 1F2h | FFh | Set Configuration Subcode |
| 1F3h | FFh | Password |
| 1F4h | FFh | Password |
| 1F5h | 3Fh | Password |
| 1F6h | AXh (Drive 0) | Drive Select |
| | BXh (Drive 1) | Drive Select |
| 1F7h | F0h | Extended Command Code |

Note: In Table 6-23:
Registers 1F2h through 1F5h must contain the exact values shown above. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.
To select the drive being reconfigured, register 1F6h should be set.
For execution of the command to begin, load register 1F7h with F0h.

### 6.7.18.3 Set Configuration Without Saving to Disk

The SET CONFIGURATION WITHOUT SAVING TO DISK command is secured to prevent accidentally accessing it. To access this command, you must write the pattern shown in Table 6-24 to the Command Block Registers. The first byte, FEh, is a subcode to the extended command code F0h.

**Table 6-24** *Accessing the SET CONFIGURATION WITHOUT SAVING TO DISK Command*

| ADDRESS | VALUE | DEFINITION |
|---|---|---|
| 1F2h | FEh | Set Configuration Subcode |
| 1F3h | FEh | Password |
| 1F4h | FEh | Password |
| 1F5h | 3Fh | Password |
| 1F6h | AXh (Drive 0) | Drive Select |
| | BXh Drive 1) | Drive Select |
| 1F7h | F0h | Extended Command Code |

Note: In Table 6-24:
Registers 1F2h through 1F5h must contain the exact values shown above. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.
To select the drive being reconfigured, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

### 6.7.18.4 Configuration Command Data Field

A 512-byte data field is associated with this command. This data field is sent to the drive through a normal 512-byte write handshake. Table 6-25 shows the format of the data field. Bytes 0 through 31 of the data field contain additional KEY information. The drive issues the message ILLEGAL COMMAND if this information is not entered correctly. Bytes 32 through 35 control the operation of DisCache. Bytes 36 through 38 control operation of the error recovery procedure. The drive does not use bytes 40 through 511, which should be set to 0.

**Table 6-25** *Configuration Command Format*

| BYTE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0–31 | QUANTUM CONFIGURATION KEY | | | | | | | |
| 32 | RESERVED = 0 | | | | | | PE | CE |
| 33 | RESERVED | | | | | | | |
| 34 | RESERVED = 0 | | | | | | | |
| 35 | RESERVED = 0 | | | | | | | |
| 36 | AWRE | ARR | N/A | RC | EEC | N/A | N/A | DCR |
| 37 | NUMBER OF RETRIES | | | | | | | |
| 38 | ECC CORRECTION SPAN | | | | | | | |
| 39 | RESERVED = 0 | | | | | WCE | RUEE | 0 |
| 40–511 | RESERVED = 0 | | | | | | | |

Note: All fields marked RESERVED or N/A should be set to zero.

### 6.7.18.5 Quantum Configuration Key (Bytes 0-31)

Bytes 0–6 must contain the ASCII characters *Q, U, A, N, T, U,* and *M*; byte 7, the ASCII character *space*; and bytes 8–20 must contain the ASCII characters *C, O, N, F, I, G, U, R, A, T, I, O,* and *N*. Bytes 21–31 must contain an ASCII *space*. If this information is not entered correctly, the drive aborts the COMMAND.

### 6.7.18.6 DisCache Parameters

**PE – Prefetch Enable (Byte 32, Bit 1):** When set to 1, this bit indicates that the drive will perform prefetching. A PE bit set to 0 indicates that no prefetching will occur. The CE bit (bit 0) must be set to 1 to enable use of the PE bit. The default value is 1.

**CE – Cache Enable (Byte 32, Bit 0):** When set to 1, this bit indicates that the drive will activate caching on all READ commands. With the CE bit set to 0, the drive will disable caching and use the RAM only as a transfer buffer. The default setting is 1.

### 6.7.18.7 Error Recovery Parameters

**AWRE – Automatic Write Reallocation Enabled (Byte 36, Bit 7):** When set to 1, indicates that the drive will enable automatic reallocation of bad blocks. Automatic Write Reallocation is similar to the function of Automatic Read Reallocation, but is initiated by the drive when a defective block has become inaccessible for writing. An AWRE bit set to 0 indicates that the Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT drives will not automatically reallocate bad blocks. The default setting is 1.

**ARR – Automatic Read Reallocation (Byte 36, Bit 6):** When set to 1, this bit indicates that the drive will enable automatic reallocation of bad sectors. The drive initiates reallocation when the ARR bit is set to 1 and the drive encounters a hard error—that is, if the triple-burst ECC algorithm is invoked. The default setting is 1. When the ARR bit is set to 0, the drive will not perform automatic reallocation of bad sectors. If RC (byte 36, bit 4) is 1, the drive ignores this bit. The default value is 1.

**RC – Read Continuous (Byte 36, Bit 4):** When set to 1, this bit instructs the drive to transfer data of the requested length without adding delays to increase data integrity—that is, delays caused by the drive's error-recovery procedures. With RC set to 1 to maintain a continuous flow of data and avoid delays, the drive may send data that is erroneous. When the drive ignores an error, it does *not* post the error. The RC bit set to 0 indicates that potentially time-consuming operations for error recovery are acceptable during data transfer. The default setting is 0.

**EEC – Enable Early Correction (Byte 36, Bit 3):** When set to 1, this bit indicates that the drive will use its ECC algorithm if it detects two consecutive equal, nonzero error syndromes. The drive will not perform rereads before applying correction, unless it determines that the error is uncorrectable. An EEC bit set to 0 indicates that the drive will use its normal recovery procedure when an error occurs: rereads, followed by error correction. If the RC bit (byte 36, bit 4) is set to 1, the drive ignores the EEC bit. The default setting is 1.

**DCR – Disable Correction (Byte 36, Bit 0):** When set to 1, this bit indicates that all data will be transferred without correction, even if it would be possible to correct the data. A DCR bit set to 0 indicates that the data will be corrected if possible. If the data is uncorrectable, it will be transferred without correction, though the drive will attempt rereads. If RC (byte 36, bit 4) is set to 1, the drive ignores this bit. The default setting is 0. The drive will post all errors, whether DCR is set to 0 or 1.

**NUMBER OF RETRIES (Byte 37):** This byte specifies the number of times that the drive will attempt to recover from data errors by rereading the data, before it will apply correction. The drive performs rereads before ECC correction—unless EEC (byte 36, bit 3) is set to 1, enabling early correction. The default is eight.

**ECC CORRECTION SPAN (Byte 38):** This byte specifies the maximum number of bits per interleave that can be corrected using triple-burst ECC. The value for this byte is fixed at 24.

#### 6.7.18.8 Drive Parameters

**WCE – Write Cache Enable (Byte 39, Bit 2):** When this bit is set to 1, the Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives enable the Write Cache. This indicates that the drive returns GOOD status for a write command after successfully receiving the data, but before writing it to the disk. A value of zero indicates that the drive returns GOOD status for a write command after successfully receiving the data and writing it to the disk.

If the next command is another WRITE command, cached data continues to be written to the disk while new data is added to the buffer. The default setting is 1.

**RUEE – Reallocate Uncorrectable Error Enables (Byte 39, Bit 1):** When set to 1, this bit indicates that the Quantum Fireball TM series of hard disk drives will automatically reallocate uncorrectable hard errors, if the ARR bit (byte 36, bit 6) is set to 1. The default setting is 1.

## 6.8 ERROR REPORTING

At the start of a command's execution, the Quantum Fireball TM 1.0/1.2/1.7/2.1/2.5/3.2/3.8AT hard disk drives check the Command Register for any conditions that would lead to an abort command error. The drive then attempts execution of the command. Any new error causes execution of the command to terminate at the point at which it occurred. Table 6-26 lists the valid errors for each command.

**Table 6-26** *Command Errors*

| COMMAND | ERROR REGISTER | | | | | | STATUS REGISTER | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | BBK | UNC | IDNF | ABRT | TKO | AMNF | DRDY | DWF | DSC | CORR | ERR |
| Check Power Mode | | | | V | | | V | V | V | | V |
| Read Defect List | V | V | V | V | | V | V | V | V | V | V |
| Execute Drive Diag. | | | | | | | | | | | V |
| Format Track | | | V | V | | | V | V | V | | V |
| Identify Drive | | | | V | | | V | V | V | | V |
| Initialize Parameters | | | | | | | V | V | V | | |
| Invalid Cmnd. Codes | | | | V | | | V | V | V | | V |
| Read Buffer | | | | V | | | V | V | V | | V |
| Read DMA | V | V | V | V | | V | V | V | V | V | V |
| Read Configuration | V | V | V | V | | V | V | V | V | V | V |
| Read Multiple | V | V | V | V | | V | V | V | V | V | V |
| Read Sectors | V | V | V | V | | V | V | V | V | V | V |
| Read Sectors Long | V | | V | V | | V | V | V | V | | V |
| Read Verify Sectors | V | V | V | V | | V | V | V | V | V | V |
| Recalibrate | | | | V | V | | V | V | V | | V |
| Seek | | | V | V | | | V | V | V | | V |
| Set Configuration | V | | V | V | | | V | V | V | | V |
| Set Features | | | | V | | | V | V | V | | V |
| Set Multiple Mode | | | | V | | | V | V | V | | V |
| Write Buffer | | | | V | | | V | V | V | | V |
| Write DMA | V | | V | V | | | V | V | V | | V |
| Write Multiple | V | | V | V | | | V | V | V | | V |
| Write Sectors | V | | V | V | | | V | V | V | | V |
| Write Sectors Long | V | | V | V | | | V | V | V | | V |

Note:
V = Valid errors for each command
ABRT = Abort command error
AMNF= Data address mark not found error
BBK = Bad block detected
CORR = Corrected data error
DRDY = Drive ready
DSC = Disk seek complete not detected
DWF = Drive write fault detected
ERR = Error bit in the Status Register
IDNF = Requested ID not found
TK0 = Track zero not found error
UNC = Uncorrectable data error